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(54) Binary Multiplication Cell Circuit

(57) A binary multiplier includes a staggered array of multiplier cells each including a NOR circuit (1) for obtaining a partial product of one binary digit of a multiplicand x_i and one binary digit, of a multiplier y_i and a full adder arranged to produce from a) the partial product, b) an augend digit from the preceding row of the array, and c) a carry digit from the preceding cell in the same row, new carry and augend (or product) digits. The full adder comprises two AND circuits (2, 8), three NOR circuits (3, 4, 9), an inverter (7) and an exclusive OR circuit (5, 6) arranged as shown. Preferably, the exclusive OR circuit is constituted by an exclusive NOR circuit (5) and an inverter (6). The arrangement reduces the number of transistors required for each cell and thus facilitates production as an integrated circuit.

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

FIG. 3

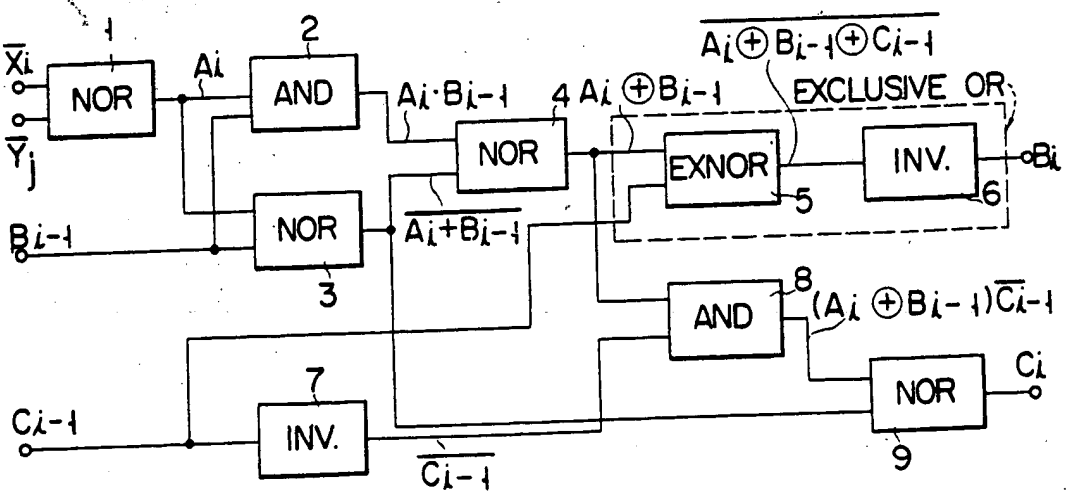

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FIG. 3

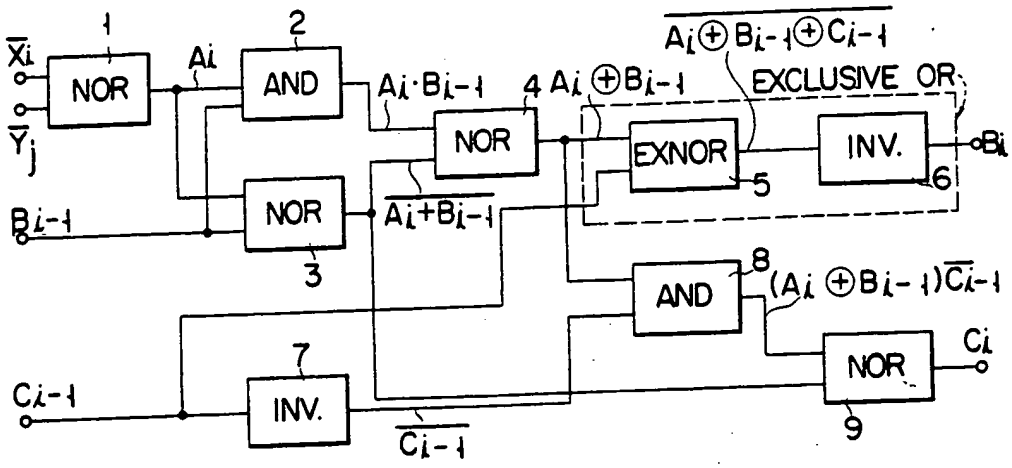
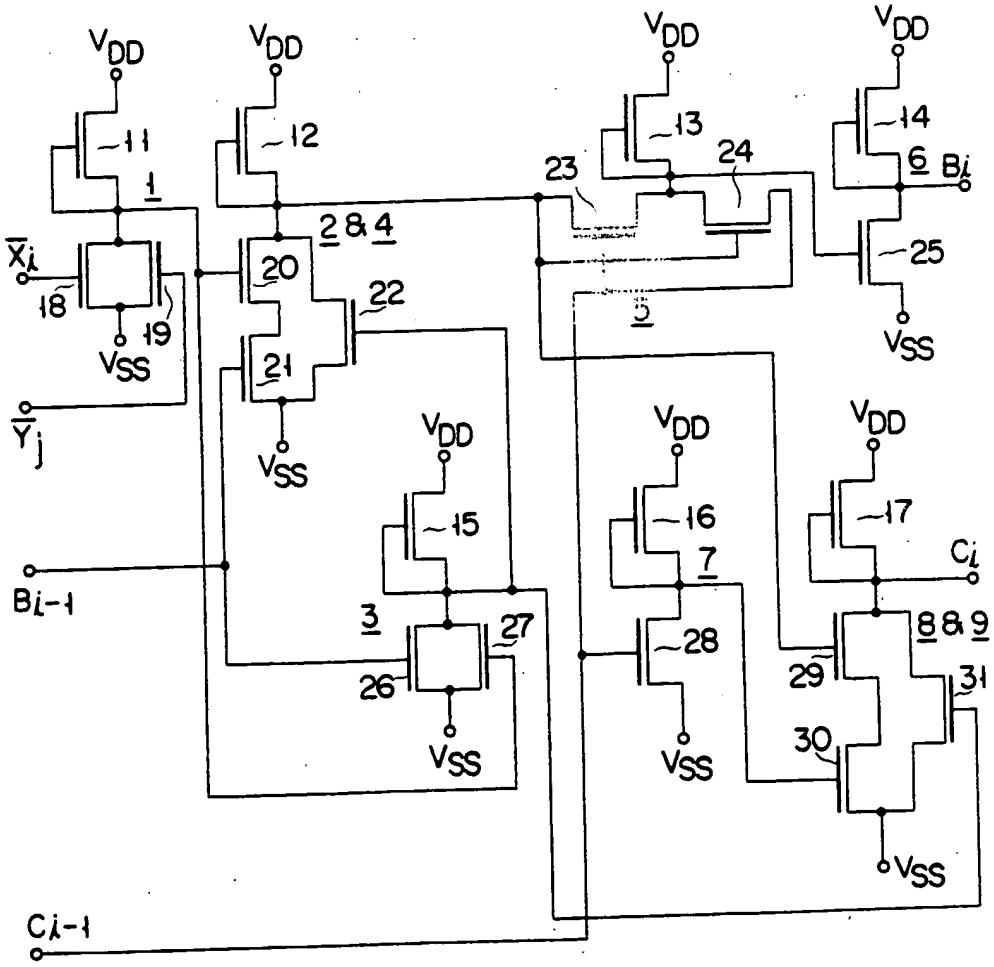


FIG. 4



binary multiplication cell circuit.

Carry digit Ci may be expressed as follows:

$$Ci=\overline{\overline{Ai}\cdot\overline{Bi-1}+Ai\cdot\overline{Bi-1}\cdot\overline{Ci-1}+\overline{Ai}\cdot Bi-1\cdot\overline{Ci-1}}$$

$$=\overline{\overline{Bi-1}(\overline{Ai}+\overline{Ci-1})+\overline{Ai}(\overline{Bi-1}+\overline{Ci-1})}$$

$$=\overline{\overline{Ai}\cdot\overline{Bi-1}+\overline{Ai}\cdot\overline{Ci}\cdot 1+\overline{Bi-1}\cdot\overline{Ci-1}}$$

$$=(Ai+Bi-1)(Ai+Ci-1)(Bi-1+Ci-1)$$

$$=Ai\cdot Bi-1+Bi-1\cdot Ci-1+Ci-1\cdot Ai$$

Fig. 4 is a circuit diagram of the binary multiplication cell circuit of Fig. 1, which is formed of N-channel insulated gate field effect transistors. The cell circuit comprises depletion load transistors 11 to 17 and enhancement transistors 18 to 31. The NOR circuit 1 is comprised of the transistors 11. 18 and 19, the NOR circuit 3 is comprised of the transistors 15, 26 and 27, the exclusive NOR circuit 5 is comprised of the transistors 13, 23 and 24, the inverter 6 is comprised of the transistors 14 and 25, and the inverter 7 is comprised of transistors 16 and 28. The AND circuit 2 and the NOR circuit 4 are constituted by the transistors 12, 20, 21 and 22. The AND circuit 8 and the NOR circuit 9 is comprised of the transistors 17, 29, 30 and 31.

The circuit of Fig. 3, except for the NOR circuit 1 which produces a partial product Ai, constitutes a full adder. If a binary multiplication cell circuit is to be comprised of one NOR circuit for producing a partial product and two typical half-adders constituting a full adder, approximately 30 transistors will be required. By contrast, the binary multiplication cell circuit shown in Fig. 4 requires but 21 transistors.

In the above-mentioned embodiment of this invention the power dissipation can be reduced without using more transistors, only if the inverters 6 and 7 are replaced each by a two-transistor complementary inverter.

Claims

1. A binary multiplication cell circuit comprising:

a first NOR circuit for providing a partial product of one binary digit of a multiplicand and one binary digit of a multiplier;

a first AND circuit connected to receive an output signal of said first NOR circuit and an augend;

a second NOR circuit connected to receive said augend and the output signal of said first NOR circuit;

a third NOR circuit connected to receive an output signal of said first AND circuit and an output signal of said second NOR circuit;

an inverter for inverting a carry binary digit;

a second AND circuit connected to receive an output signal of said first inverter and an output signal of said third NOR circuit;

a fourth NOR circuit connected to receive an output signal of said second AND circuit and the output signal of said second NOR circuit; and

an exclusive OR circuit connected to receive the carry binary digit and the output signal of said third NOR circuit.

2. A binary multiplication cell circuit according to claim 1, wherein said exclusive OR circuit is constituted by an exclusive NOR circuit and an inverter.

3. A binary multiplication cell circuit, substantially as hereinbefore described with reference to the accompanying drawings.

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